BEILSTEIN JOURNAL OF NANOTECHNOLOGY

High–low Kelvin probe force spectroscopy for measuring the interface state density

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Full Research Paper

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Keywords:
high–low Kelvin probe force microscopy; high–low Kelvin probe force spectroscopy; interface state density; Kelvin probe force microscopy; Kelvin probe force spectroscopy

Beilstein J. Nanotechnol. **2023,** *14,* 175–189.
https://doi.org/10.3762/bjnano.14.18

Received: 09 September 2022
Accepted: 19 January 2023
Published: 31 January 2023

Associate Editor: T. Glatzel

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Abstract

The recently proposed high–low Kelvin probe force microscopy (KPFM) enables evaluation of the effects of semiconductor interface states with high spatial resolution using high and low AC bias frequencies compared with the cutoff frequency of the carrier transfer between the interface and bulk states. Information on the energy spectrum of the interface state density is important for actual semiconductor device evaluation, and there is a need to develop a method for obtaining such physical quantities. Here, we propose high–low Kelvin probe force spectroscopy (high–low KPFS), an electrostatic force spectroscopy method using high- and low-frequency AC bias voltages to measure the interface state density inside semiconductors. We derive an analytical expression for the electrostatic forces between a tip and a semiconductor sample in the accumulation, depletion, and inversion regions, taking into account the charge transfer between the bulk and interface states in semiconductors. We show that the analysis of electrostatic forces in the depletion region at high- and low-frequency AC bias voltages provides information about the interface state density in the semiconductor bandgap. As a preliminary experiment, high-low KPFS measurements were performed on ion-implanted silicon surfaces to confirm the dependence of the electrostatic force on the frequency of the AC bias voltage and obtain the interface state density.

Introduction

With the recent miniaturization of semiconductor devices, understanding the physical and electrical properties of semiconductor devices, such as the dopant concentration, dopant distribution, and defect level distribution, at the nanoscale has become important. Among the physical properties of semiconductors, information on semiconductor interface states is particularly important. For example, in semiconductor devices such as field-effect transistors, the presence of semiconductor interface states is known to significantly affect device operation characteristics [1-3]. Therefore, direct observation of semicon-

ductor surfaces with nanoscale spatial resolution will become even more important for understanding and controlling the effects of these properties on devices and for evaluating semiconductor device operation.

Kelvin probe force microscopy (KPFM) is known as a method that can measure the contact potential difference (CPD) between a tip and a sample with high spatial resolution [4,5]. KPFM is based on the detection of the electrostatic force between a tip and a sample using atomic force microscopy (AFM) [6-8]. CPD and topographic measurements have been performed on a variety of sample surfaces, including metals [9,10], semiconductors [11-14], and insulators [15-17]. When a semiconductor sample is measured by KPFM, the measured CPD is related to information about the semiconductor properties such as dopant density, surface charge, band bending, and interface state density [18]. In particular, previous studies of silicon substrates with different impurity concentrations measured by KPFM have shown that when the impurity concentration is very high ($>10^{16}$ cm^{-3}), surface band bending occurs, and the measured CPD approaches that of the intrinsic semiconductor [19]. Thus, since the CPD is strongly affected by the surface properties, accurate evaluation of the surface state and bulk impurity concentration requires a method that extracts only the surface potential effect due to interface states.

Recently, we proposed high–low Kelvin probe force microscopy (high–low KPFM) as a technique to solve the above problem [20,21]. High–low KPFM is a method for measuring the magnitude and direction of band bending due to interface states by applying low-frequency and high-frequency AC bias voltages between the tip and the sample with respect to the cutoff frequency f_c of carrier transport between the bulk and interface states and measuring the difference in CPD by KPFM. In high–low KPFM, frequency modulation (FM) KPFM (FM-KPFM) combined with FM-AFM is used to detect the tip–sample interaction force. FM-KPFM has several advantages, namely high sensitivity to the electrostatic force gradient, high detection sensitivity using a cantilever with a weak spring constant at the first resonance, ease of implementation in adding FM-AFM, and no need to enhance the bandwidth of the cantilever deflection sensor. FM-KPFM is used to apply an AC bias voltage at frequencies lower than the cutoff frequency f_c of carrier transport, and heterodyne FM-KPFM, based on the heterodyne effect (frequency conversion effect) between mechanical oscillation of the cantilever and electrostatic force oscillation, is used to apply an AC bias voltage at frequencies higher than the cutoff frequency f_c of carrier transport. To date, high–low KPFM has successfully visualized the surface band bending of pn-patterned silicon substrates [22]. However, in high–low KPFM, the CPD is compensated by a DC bias voltage. Hence, a certain DC voltage, determined by the CPD, is applied to the semiconductor sample. Therefore, the surface potential of the semiconductor is fixed at a certain energy, and only the surface state near the Fermi level of the surface is reflected in CPD measurements, making measurement of the energy distribution of the interface states within the bandgap difficult. Thus, a method for measuring the energy distribution of the interface states must be developed.

Kelvin probe force spectroscopy (KPFS) or electrostatic force spectroscopy is a technique that enables energy spectroscopy of interface states in the semiconductor bandgap, as described above. Since KPFS does not fix the DC bias voltage but sweeps it over a certain voltage range, it has the advantage of obtaining information on carriers in the energy range corresponding to the swept bias voltage range. For example, the use of electrostatic force spectroscopy to measure the localized energy levels of insulating layers on semiconductor surfaces has been reported to be feasible [22]. Therefore, we can expect that the KPFS method described above can be combined with high–low KPFM to measure the energy distribution of the interface states.

In this study, we propose high-low KPFS using high- and low-frequency AC bias voltages to measure the interface state density inside semiconductors. We derive an analytical expression for the electrostatic force between the tip and the sample that takes into account the charge transfer between the bulk and interface states in the semiconductor. We show that the electrostatic force between the tip and the semiconductor sample strongly depends on the capacitance of the charge depletion region on the surface, and that the analysis of the electrostatic force at low- and high-frequency AC bias voltages can provide information on the interface state density in the semiconductor bandgap. We also demonstrate using a pn-patterned silicon substrate that the interface state density can be measured.

Theory

To understand the principle of the high–low KPFS proposed in this study, we discuss the electrostatic forces acting between the tip and the sample when high- and low-frequency AC bias voltages are applied. The tip and the sample are assumed to be metallic and semiconducting, respectively, and a metal–insulator–semiconductor (MIS) structure consisting of the metallic tip, a vacuum gap, and the semiconducting sample is considered (Figure 1a). No oxide film on the semiconductor surface is assumed, and to simplify the discussion, the CPD between the tip and the semiconductor substrate is assumed to be zero.

To investigate the electrostatic force acting between the tip and the semiconductor surface, we use the theoretical model reported by Hudlet and co-workers [23]. For simplicity, let us

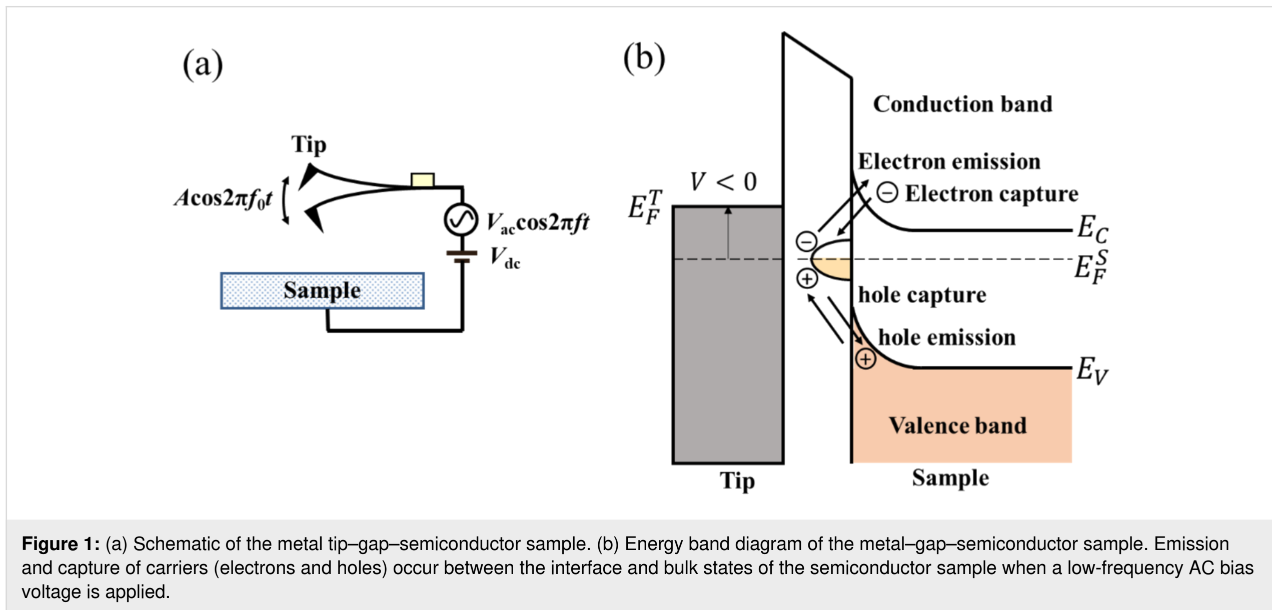

Figure 1: (a) Schematic of the metal tip–gap–semiconductor sample. (b) Energy band diagram of the metal–gap–semiconductor sample. Emission and capture of carriers (electrons and holes) occur between the interface and bulk states of the semiconductor sample when a low-frequency AC bias voltage is applied.

assume that the tip and the sample are represented by parallel plate capacitors. In this case, the electrostatic force F_{ele} acting between the tip and the semiconductor surface is expressed as

$$F_{ele} = -\frac{Q^2}{2\varepsilon_0}, \quad (1)$$

where Q is the charge per unit surface area induced on the semiconductor surface and ε_0 is the dielectric constant of vacuum.

A bias voltage $V_{dc} + V_{ac} \cdot \cos 2\pi ft$ is applied between the tip and the semiconductor sample, where V_{dc}, V_{ac}, and f are the DC bias voltage, amplitude of the AC bias voltage, and modulation frequency of the AC bias voltage, respectively. The modulated electrostatic force $F_{ele}(f)$ between the tip and the surface is expressed as follows using Taylor series expansion:

$$\begin{aligned} F_{ele}(f) &= -\frac{dF_{ele}}{dV} V_{ac} \cos 2\pi ft \\ &= -\frac{dF_{ele}(Q)}{dQ} \frac{dQ}{dV_s} \frac{dV_s}{dV} V_{ac} \cos 2\pi ft, \end{aligned} \quad (2)$$

where V_s is the surface potential of the semiconductor sample.

Next, we consider the charge Q induced on the semiconductor surface. When a bias voltage is applied between a metal tip and a semiconductor surface, a surface potential is generated on the semiconductor surface, resulting in, for example, surface charge accumulation, depletion, and inversion states. The relationship between this surface charge and the electrostatic force between the tip and the sample has already been discussed by Hudlet and co-workers [23]. Additionally, there are interface states on the semiconductor surface. Therefore, the contribution of these interface states to the AC component of the electrostatic force must be considered. When an AC bias voltage is applied between the tip and the sample, the bulk Fermi level does not change on the semiconductor side, whereas the interface states move up and down with the conduction and valence bands. This causes capture of carriers (electrons and/or holes) from the bulk side by the interface states and, conversely, emission of carriers from the interface states to the bulk side, which contribute to the electrostatic force (Figure 1b). Therefore, the total charge Q induced on the semiconductor surface by the voltage application is given by the sum of the charge Q_s due to the surface potential V_s and the charge Q_{it} due to the interface states as follows:

$$Q = Q_s + Q_{it}. \quad (3)$$

Here, we consider the charge Q_s due to the surface potential V_s. In the case of an n-type semiconductor, the charge Q_s as a function of the surface potential V_s is expressed as follows [23,24]:

$$Q_s = -\mathrm{sgn}(u) \frac{k_B T}{e} \frac{\varepsilon}{L_D} F(u), \quad (4)$$

$$F(u) = \left[\left(\exp(u) - u - 1 \right) + \frac{n_i^2}{N_D^2} \left(\exp(-u) + u - 1 \right) \right]^{\frac{1}{2}}, \quad (5)$$

$$u = \frac{eV_s}{k_B T}, \quad (6)$$

$$L_\mathrm{D} = \left(\frac{\varepsilon k_\mathrm{B} T}{2 N_\mathrm{D} e^2} \right)^{1/2}, \tag{7}$$

where N_D is the dopant density, n_i is the intrinsic carrier density, and ε is the dielectric constant. L_D is the Debye length for majority carriers (electrons), which characterizes the change in the potential inside the semiconductor. k_B, T and e are the Boltzmann constant, absolute temperature, and elementary charge ($e > 0$), respectively.

Since the applied voltage V is divided between the semiconductor and the gap, the following equation is obtained:

$$V = V_\mathrm{s} - \frac{Q_\mathrm{s}(V_\mathrm{s})}{C_\mathrm{g}}, \tag{8}$$

where C_g is the capacitance per unit surface area due to the gap between the tip and the surface. The charge Q_s due to the surface potential V_s is obtained by numerically solving Equations 4–8.

When a positive or negative bias voltage is applied to the MIS structure consisting of the metal tip, gap, and semiconductor sample, three cases exist at the semiconductor surface. For an n-type semiconductor, when a positive bias voltage is applied to the metal tip ($V_\mathrm{dc} > 0$), electrons (majority carriers) in the semiconductor are attracted to the surface, forming an accumulation layer of electrons. When a small negative bias voltage is applied to the metal tip ($V_\mathrm{dc} < 0$), electrons (majority carriers) in the semiconductor are depleted from the surface, forming a depletion layer. When a large negative bias voltage is applied to the metal tip, the number of holes (minority carriers) is greater than that of electrons at the surface, and holes are induced in the semiconductor at the surface, forming an inversion layer of holes.

Here, in the accumulation region, since $N_\mathrm{D}^2 \gg n_i^2$ and $\exp(u) \gg |u + 1|$, Q_s is dominated by the first term in Equation 5 and is given by [23,24]

$$Q_\mathrm{s}(0) = -\frac{k_\mathrm{B} T}{e} \frac{\varepsilon}{L_\mathrm{D}} \exp\left(\frac{e V_\mathrm{s}}{2 k_\mathrm{B} T} \right). \tag{9}$$

In the depletion region, Q_s is dominated by the second term $-u$ in the square brackets on the right-hand side of Equation 5 and is given by

$$Q_\mathrm{s}(0) = \frac{\varepsilon}{L_\mathrm{D}} \left(\frac{k_\mathrm{B} T}{e} \right)^{\frac{1}{2}} \sqrt{|V_\mathrm{s}|}. \tag{10}$$

In the strong inversion region, Q_s is dominated by the fourth term $n_i^2 / N_\mathrm{D}^2 \cdot \exp(-u)$ in the square brackets on the right-hand side of Equation 5 and is given by

$$Q_\mathrm{s}(0) = \frac{\varepsilon k_\mathrm{B} T}{e L_\mathrm{D}} \left(\frac{n_i^2}{N_D^2} \right)^{1/2} \exp\left(\frac{e |V_\mathrm{s}|}{2 k_\mathrm{B} T} \right). \tag{11}$$

Similar results can be obtained for a p-type semiconductor.

Next, we consider the charge Q_it due to the interface states. In indirect-bandgap semiconductors such as Si with a low carrier density below 10^{17} cm^{-3}, the charge (electron and hole) transfer between the interface and bulk states at low carrier density can be explained by the model with Shockley–Read–Hall (SRH) statistics [25,26]. This model is based on the charge capture and emission between the interface and bulk states (Figure 2). Assume that $C_\mathrm{cn}^\mathrm{SRH}$ and $C_\mathrm{cp}^\mathrm{SRH}$ are the capture rates for electrons and holes per electron and hole, respectively, when all interface states are unoccupied, and $C_\mathrm{en}^\mathrm{SRH}$ and $C_\mathrm{ep}^\mathrm{SRH}$ are the emission rates for electrons and holes per electron and hole, respectively. The capture rates per unit volume for electrons and holes (R_n^SRH and R_p^SRH) are given by [25,26]

$$R_n^\mathrm{SRH} = C_\mathrm{cn}^\mathrm{SRH} \cdot n \cdot (1 - f_\mathrm{it}), \tag{12}$$

$$R_p^\mathrm{SRH} = C_\mathrm{cp}^\mathrm{SRH} \cdot p \cdot f_\mathrm{it}, \tag{13}$$

where f_it is the fraction of occupied interface states. n and p are the electron and hole densities of the bulk state. Analogously, the emission rates per unit volume for electrons and holes (G_n^SRH and G_p^SRH) are given by

$$G_n^\mathrm{SRH} = C_\mathrm{en}^\mathrm{SRH} \cdot f_\mathrm{it}, \tag{14}$$

$$G_p^\mathrm{SRH} = C_\mathrm{ep}^\mathrm{SRH} \cdot (1 - f_\mathrm{it}). \tag{15}$$

In thermal equilibrium, the amount of capture and the amount of emission for a carrier coincide as follows:

$$R^\mathrm{SRH} = R_n^\mathrm{SRH} - G_n^\mathrm{SRH} = R_p^\mathrm{SRH} - G_p^\mathrm{SRH}. \tag{16}$$

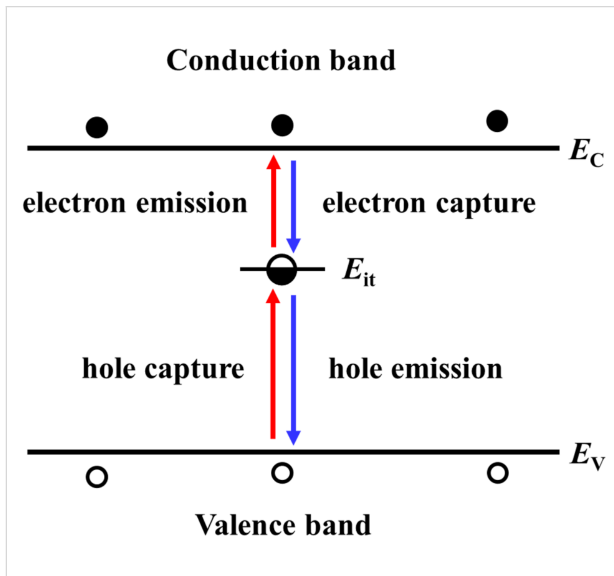

Figure 2: Schematic model of carrier emission and capture between the interface and bulk states of the semiconductor sample.

The net generation/recombination rate R^{SRH} is given by the following equation [25,26]:

$$R^{SRH} = \frac{np - n_i^2}{\tau_p\left(n + n_1\right) + \tau_n\left(p + p_1\right)}, \quad (17)$$

with

$$n_1 = n_0 \frac{1 - f_{it0}}{f_{it0}}, \quad (18)$$

$$p_1 = p_0 \frac{f_{it0}}{1 - f_{it0}}. \quad (19)$$

The index 0 indicates equilibrium quantities. For low-level injection, at which the excess minority carrier density is low compared to the equilibrium majority carrier density, the net generation/recombination rate R^{SRH} is dominated by the hole (minority carrier) lifetime τ_p in n-type semiconductors and the electron (minority carrier) lifetime τ_n in p-type semiconductors as follows:

$$\tau_p = \frac{1}{C_{pn}^{SRH}} = \frac{1}{\sigma_p v_{th} N_{it}}, \quad (20)$$

$$\tau_n = \frac{1}{C_{cn}^{SRH}} = \frac{1}{\sigma_n v_{th} N_{it}}, \quad (21)$$

where σ_n and σ_p are the capture cross sections for electrons and holes, respectively, v_{th} is the thermal velocity, and N_{it} is the concentration of interface states. These equations indicate that the carrier lifetimes τ_p and τ_n are reciprocals of the capture rates per single carrier determined by the capture cross sections σ_n and σ_p, thermal velocity v_{th}, and concentration of interface states N_{it}, which depend on semiconductor type, temperature, carrier density, and interface state density.

For an n-type Si semiconductor at room temperature, the hole (minority carrier) lifetime τ_p as a function of electron (majority carrier) density n has been experimentally investigated and is reported to be less than 2.5×10^{-5} s for low carrier densities $n < 5 \times 10^{17}$ cm^{-3} [26]. Additionally, for metal-oxide semiconductor capacitors on Si(100) substrates, the lifetimes τ_n and τ_p as functions of the sum of the surface potential and the Fermi potential with respect to the midgap have been experimentally investigated [24]. As a result, for Si semiconductors with a low carrier density (small Fermi potential), the lifetime has been reported to be less than 5×10^{-6} s. These results indicate that the cutoff frequency f_c of carrier transport between the interface and bulk states for a Si substrate with a low carrier density is approximately 200 kHz. Therefore, when an AC bias voltage with a frequency higher than this cutoff frequency f_c is applied between the tip and the Si semiconductor sample, the charge Q_{it} caused by the interface states cannot respond to changes in the surface potential. In contrast, when an AC bias voltage with a frequency much lower than f_c is applied between the tip and the Si semiconductor sample, the charge Q_{it} can respond to changes in the surface potential.

Low KPFS

First, we consider the case in which the frequency of the AC bias voltage is lower than the cutoff frequency f_c of the carrier transport between the interface and bulk states. The AC bias voltage $V_{ac} \cdot \cos 2\pi f_m t$ is applied between the tip and the surface, where f_m is the modulation frequency of the AC bias voltage. Since the charge Q_{it} due to interface states can follow the change in the surface potential, dQ/dV_s and dV_s/dV can be expressed as

$$\frac{dQ}{dV_s} = \frac{d\left(Q_s + Q_{it}\right)}{dV_s} = -\left(C_D + C_{it}\right), \quad (22)$$

$$\frac{dV_s}{dV} = \frac{C_g}{C_g + C_D + C_{it}}, \quad (23)$$

where C_D and C_{it} are the capacitance per unit surface area due to the depletion layer of the semiconductor and the capacitance

due to the interface charge, respectively. The applied voltage is divided between the semiconductor and the gap, and the following equation is obtained:

$$V_{\mathrm{dc}} = V_{\mathrm{s}} - \frac{Q_{\mathrm{s}} + Q_{\mathrm{it}}}{C_{\mathrm{g}}}. \tag{24}$$

Therefore, the modulation frequency f_{m} component of the electrostatic force $F_{\mathrm{ele}}(f_{\mathrm{m}})$ acting on the probe is expressed as

$$\begin{aligned} F_{\mathrm{ele}}\left(f_{\mathrm{m}}\right) &= \frac{Q_{\mathrm{s}} + Q_{\mathrm{it}}}{\varepsilon_0} \frac{C_{\mathrm{g}}\left(C_{\mathrm{D}} + C_{\mathrm{it}}\right)}{C_{\mathrm{g}} + C_{\mathrm{D}} + C_{\mathrm{it}}} V_{\mathrm{ac}} \cos 2\pi f_{\mathrm{m}} t \\ &= \frac{C_{\mathrm{g}}\left(V_{\mathrm{s}} - V_{\mathrm{dc}}\right)}{\varepsilon_0} C_{\mathrm{LF}} V_{\mathrm{ac}} \cos 2\pi f_{\mathrm{m}} t, \end{aligned} \tag{25}$$

$$C_{\mathrm{LF}} = \frac{C_{\mathrm{g}}\left(C_{\mathrm{D}} + C_{\mathrm{it}}\right)}{C_{\mathrm{g}} + C_{\mathrm{D}} + C_{\mathrm{it}}}, \tag{26}$$

where C_{LF} is the low-frequency tip–sample capacitance. The equivalent circuit for this capacitance C_{LF} is shown in Figure 3b. Note that this equivalent circuit is equal to the equivalent circuit of the impedance model (SRH model) of the MIS structure (Figure 3a), neglecting the resistance component R_{it}. This result suggests a similarity between conventional impedance measurements and electrostatic force measurements in semiconductor surface and interface evaluation techniques.

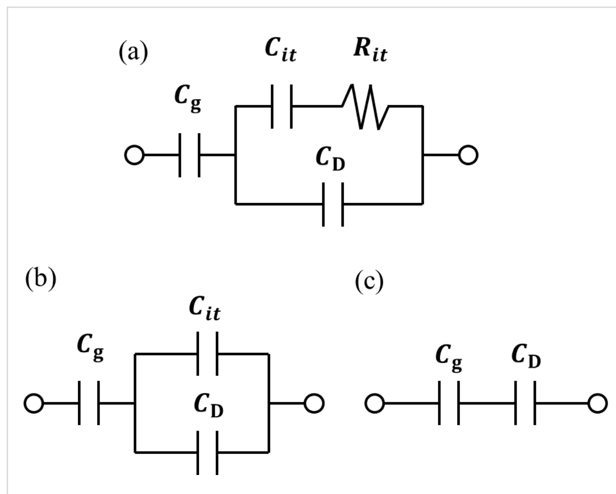

Figure 3: (a) Equivalent circuit of the impedance model (SRH model) of the MIS structure. (b) Equivalent circuit of tip–sample capacitance C_{LF} in low-frequency KPFS with a low-frequency AC bias voltage. (c) Equivalent circuit of tip–sample capacitance C_{HF} in high-frequency KPFS with a high-frequency AC bias voltage. C_{g}: capacitance due to the tip–surface gap; C_{D}: capacitance due to the depletion layer; C_{it}: capacitance due to interface states; R_{it}: resistance due to interface states.

The average distance between the tip and the sample is z_{to}, and the amplitude and frequency of the vibrating cantilever are A and f_0, respectively. The time-varying tip–sample distance is given by

$$z = z_{\mathrm{to}} + A \cos 2\pi f_0 t. \tag{27}$$

From this equation and the relationship $C_{\mathrm{g}} = \varepsilon_0/z$, we obtain the following expression:

$$\begin{aligned} \frac{\partial}{\partial z}\left[\frac{C_{\mathrm{g}}}{\varepsilon_0} C_{\mathrm{LF}}\right] &\approx -\left(C_{\mathrm{D}} + C_{\mathrm{it}}\right)\left[\frac{1}{z_{\mathrm{to}}^{2}} - \frac{1}{\left(z_{\mathrm{to}} + \frac{\varepsilon_0}{C_{\mathrm{D}} + C_{\mathrm{it}}}\right)^2}\right] \\ &\cdot A \cos 2\pi f_0 t. \end{aligned} \tag{28}$$

Because of frequency mixing between the electrostatic force due to the AC bias voltage $\cos 2\pi f_{\mathrm{m}} t$ and the cantilever vibration $\cos 2\pi f_0 t$, $f_0 \pm f_{\mathrm{m}}$ components of the electrostatic force $F_{\mathrm{ele},L}(f_0 \pm f_{\mathrm{m}})$ appear:

$$\begin{aligned} F_{\mathrm{ele},L}\left(f_0 \pm f_{\mathrm{m}}\right) &= -\frac{1}{2}\left(C_{\mathrm{D}} + C_{\mathrm{it}}\right)\left[\frac{1}{z_{\mathrm{to}}^{2}} - \frac{1}{\left(z_{\mathrm{to}} + \frac{\varepsilon_0}{C_{\mathrm{D}} + C_{\mathrm{it}}}\right)^2}\right] \\ &\cdot \left(V_{\mathrm{s}} - V_{\mathrm{dc}}\right) V_{\mathrm{ac}} A \cos 2\pi\left(f_0 \pm f_{\mathrm{m}}\right) t. \end{aligned} \tag{29}$$

When the electrostatic force is detected by the FM method, the electrostatic force $F_{\mathrm{ele},L}(f_0 \pm f_{\mathrm{m}})$ is demodulated into the f_{m} component of the frequency shift $\Delta f_L(f_{\mathrm{m}})$, which is expressed as

$$\begin{aligned} \Delta f_L\left(f_{\mathrm{m}}\right) &= -\frac{f_0}{2kA}\left[F_{\mathrm{ele},L}\left(f_0 + f_{\mathrm{m}}\right) + F_{\mathrm{ele},L}\left(f_0 - f_{\mathrm{m}}\right)\right] \\ &= \frac{f_0}{4k}\left(C_{\mathrm{D}} + C_{\mathrm{it}}\right)\left[\frac{1}{z_{\mathrm{to}}^{2}} - \frac{1}{\left(z_{\mathrm{to}} + \frac{\varepsilon_0}{C_{\mathrm{D}} + C_{\mathrm{it}}}\right)^2}\right] \\ &\cdot \left(V_{\mathrm{s}} - V_{\mathrm{dc}}\right) V_{\mathrm{ac}} \cos 2\pi f_{\mathrm{m}} t, \end{aligned} \tag{30}$$

where k is the spring constant of the cantilever. This equation indicates that the slope of the dependence of the f_{m} component of the frequency shift $\Delta f_L(f_{\mathrm{m}})$ on the DC bias voltage V_{dc} ($\Delta f_L(f_{\mathrm{m}})$–$V_{\mathrm{dc}}$ curve) is proportional to the capacitance inside the semiconductor at a low-frequency AC bias ($C_{\mathrm{D}} + C_{\mathrm{it}}$).

High KPFS

Next, we consider the case in which the frequency of the AC bias voltage is higher than the cutoff frequency f_{c} of the carrier transport between the interface and bulk states. We assume that the heterodyne FM method [21] is used and that an AC bias

voltage with a high frequency near twice the vibration frequency of the cantilever $V_{ac} \cdot \cos 2\pi(2f_0 + f_m)t$ is applied (that is, $f = 2f_0 + f_m$). In the high-frequency case, the contribution from the interface charge Q_{it} due to interface states cannot follow the change in surface potential V_s, so this contribution can be neglected. Therefore, dQ/dV_s and dV_s/dV can be expressed as

$$\frac{dQ}{dV_s} = \frac{dQ_s}{dV_s} = -C_D, \quad (31)$$

$$\frac{dV_s}{dV} = \frac{C_g}{C_g + C_D}. \quad (32)$$

Since the applied voltage is divided between the semiconductor and the gap, the following equation is obtained:

$$V_{dc} = V_s - \frac{Q_s}{C_g}. \quad (33)$$

Therefore, the modulation frequency $(2f_0 + f_m)$ component of the electrostatic force $F_{ele}(2f_0 + f_m)$ acting on the tip is expressed as

$$\begin{aligned} F_{ele}(2f_0+f_m) &= \frac{Q}{\varepsilon_0}\frac{C_g C_D}{C_g + C_D} V_{ac} \cos 2\pi(2f_0 + f_m)t \\ &= \frac{C_g(V_s - V_{dc})}{\varepsilon_0} C_{HF} V_{ac} \cos 2\pi(2f_0 + f_m)t, \end{aligned} \quad (34)$$

$$C_{HF} = \frac{C_g C_D}{C_g + C_D}, \quad (35)$$

where C_{HF} is the high-frequency tip–sample capacitance. The equivalent circuit for this capacitance C_{HF} is shown in Figure 3c. Note that this equivalent circuit is equal to the equivalent circuit of the impedance of the MIS structure derived from the SRH model (Figure 3a), neglecting the capacitance component C_{it} and resistance component R_{it} due to the semiconductor interface states.

Now, the capacitance C_D of the depletion layer of the MIS structure is given by $C_D = |dQ_s/dV_s|$. In the charge accumulation region, from Equation 9, C_D is given by

$$\begin{aligned} C_D &= \frac{\varepsilon}{L_D}\exp\left(\frac{eV_s}{k_B T}\right) \gg C_g \\ C_{HF} &\cong C_g. \end{aligned} \quad (36)$$

In the depletion region, from Equation 10, C_D is given by

$$\begin{aligned} C_D &= \frac{\varepsilon}{L_D}\left(\frac{k_B T}{e}\right)^{1/2} |V_s|^{-1/2} \ll C_g \\ C_{HF} &\cong C_D. \end{aligned} \quad (37)$$

In the inversion region, from Equation 11, C_D is given by

$$\begin{aligned} C_D &= \frac{\varepsilon}{L_D}\frac{n_i^2}{N_D^2}\exp\left(\frac{e|V_s|}{2k_B T}\right) \gg C_g \\ C_{HF} &\cong C_g. \end{aligned} \quad (38)$$

Therefore, in the depletion region, we can obtain the following expression:

$$\frac{\partial}{\partial z}\left[\frac{C_g}{\varepsilon_0} C_{HF}\right] \approx -C_D \left[\frac{1}{z_{to}^2} - \frac{1}{\left(z_{to} + \frac{\varepsilon_0}{C_D}\right)^2}\right] A\cos 2\pi f_0 t. \quad (39)$$

In the accumulation and inversion regions, we can obtain the following expression:

$$\frac{\partial}{\partial z}\left[\frac{C_g}{\varepsilon_0} C_{HF}\right] \approx -C_g \frac{1}{z_{to}^2} A\cos 2\pi f_0 t. \quad (40)$$

Because of frequency mixing between the electrostatic force due to the AC bias voltage $\cos 2\pi(2f_0 + f_m)t$ and the cantilever vibration $\cos 2\pi f_0 t$, the $f_0 + f_m$ component of the electrostatic force $F_{ele,H}(f_0 + f_m)$ appears:

- In the depletion region,

$$\begin{aligned} F_{ele,H}(f_0 + f_m) &= -\frac{1}{2} C_D \left[\frac{1}{z_{to}^2} - \frac{1}{\left(z_{to} + \frac{\varepsilon_0}{C_D}\right)^2}\right] \\ &\cdot (V_s - V_{dc}) V_{ac} A \cos 2\pi(f_0 + f_m). \end{aligned} \quad (41)$$

- In the accumulation and inversion regions,

$$F_{ele,H}(f_0 + f_m) = -\frac{1}{2} C_g \frac{1}{z_{to}^2}(V_s - V_{dc}) V_{ac} A \cos 2\pi(f_0 + f_m). \quad (42)$$

In the FM method, the electrostatic force $F_{ele,H}(f_0 + f_m)$ is demodulated into the f_m component of the frequency shift $\Delta f_H(f_m)$. The resulting f_m component of the frequency shift $\Delta f_H(f_m)$ is expressed in the depletion region as

$$\Delta f_H(f_m) = -\frac{f_0}{2kA} F_{ele,H}(f_0 + f_m) = \frac{f_0}{8k} C_D \left[\frac{1}{z_{to}^2} - \frac{1}{\left(z_{to} + \frac{\varepsilon_0}{C_D}\right)^2} \right] \cdot (V_s - V_{dc}) V_{ac} \cos 2\pi f_m t \quad (43)$$

and in the accumulation and inversion regions as

$$\Delta f_H(f_m) = -\frac{f_0}{2kA} F_{ele,H}(f_0 + f_m) = \frac{f_0}{8k} C_g \frac{1}{z_{to}^2} (V_s - V_{dc}) V_{ac} \cos 2\pi f_m t. \quad (44)$$

In the above equations, the slope of the dependence of the f_m component of the frequency shift $\Delta f_H(f_m)$ on V_{dc} ($\Delta f_H(f_m)$–V_{dc} curve) is proportional to the capacitance C_D inside the semiconductor in the depletion region and to the gap capacitance C_g in the accumulation and inversion regions. Note that at a high-frequency AC bias voltage, as shown in Equation 43 and Equation 44, only the $f_0 + f_m$ component of the electrostatic force $F_{ele,H}(f_0 + f_m)$ is demodulated, while at a low-frequency AC bias voltage, as shown in Equation 30, the $f_0 + f_m$ and $f_0 - f_m$ components of the electrostatic force $F_{ele,L}(f_0 \pm f_m)$ are demodulated. Therefore, the coefficients in Equation 43 and Equation 44 are 1/2 of those in Equation 30.

High–low KPFM

Here, we consider the derivation of the surface potential V_s induced by the interface states. When the KPFM measurement is performed using a low-frequency AC bias voltage, the DC bias voltage that makes the modulation component of the frequency shift $\Delta f_L(f_m)$ zero is

$$V_{dc} = V_{s(LF)}. \quad (45)$$

Here, $V_{s(LF)}$ can be thought of as reflecting information about the sum of the surface potential (band bending) due to the interface states and the CPD between the metal tip and the bulk state of the sample. This is because when a low-frequency AC bias voltage is used, the charge Q_{it} can respond to changes in the surface potential. In contrast, when the KPFM measurement is performed using a high-frequency AC bias voltage, the DC bias voltage that makes the modulation component of the frequency shift $\Delta f_H(f_m)$ zero is

$$V_{dc} = V_{s(HF)}. \quad (46)$$

Here, $V_{s(HF)}$ can be thought of as reflecting information about the CPD between the metal tip and the bulk state of the sample. This is because when a high-frequency AC bias voltage is used, the charge Q_{it} caused by the interface states cannot respond to changes in the surface potential. Therefore, as shown in the next equation, high–low KPFM, which measures the difference between $V_{s(LF)}$ with a low-frequency AC bias voltage and $V_{s(HF)}$ with a high-frequency AC bias voltage, reflects the information of the surface potential (band bending) due to the interface states [21,22].

$$\Delta V_s = \pm\left(V_{s(LF)} - V_{s(HF)}\right). \quad (47)$$

Regarding the selection of ±, + is for applying a bias voltage to the sample and − is for applying a bias voltage to the tip. The + and − signs of ΔV_s indicate upward and downward band bending at the interface, respectively.

High–low KPFS

Next, let us consider the derivation of the interface state density D_{it} from Equation 30 and Equation 43, which relate the modulation components of the frequency shift to the AC bias voltage at low and high frequencies. In the case of a low-frequency AC bias, from Equation 30, the slope of the $\Delta f_L(f_m)$–V_{dc} curve is proportional to the low-frequency capacitance inside the semiconductor ($C_D + C_{it}$). In the case of a high-frequency AC bias, from Equation 43, twice the slope of the $\Delta f_H(f_m)$–V_{dc} curve in the depletion region is proportional to the high-frequency capacitance within the semiconductor (C_D). Using these relationships, the interface state density D_{it} at each DC bias voltage V_{dc} can be obtained by taking the difference in the slope of the dependence of $\Delta f(f_m)$ on the DC bias voltage for low and high frequencies (the capacitance C_{it} due to the interface charge) [24] as follows:

$$D_{it} = \frac{C_{it}}{e^2} = \frac{1}{e^2}\left[\left(C_D + C_{it}\right) - C_D\right]. \quad (48)$$

Δf–V_{dc} curve with low- and high-frequency AC bias voltages

We consider the derivation of the Δf–V_{dc} curve. The DC electrostatic force $F_{ele}(0)$ between the tip and the surface when using an AC bias voltage with frequency f (= f_m or $2f_0 + f_m$) is expressed as follows using Taylor series expansion up to the second-order terms:

$$F_{ele}(0) = -\frac{Q(0)^2}{2\varepsilon_0} - \frac{1}{4} \frac{d^2 F_{ele}(f)}{dV^2} V_{ac}^2. \quad (49)$$

The contribution of the second-order terms of the Taylor series expansion of the electrostatic force is much smaller than that of the zeroth-order term and can be ignored. Q_s can be obtained by solving Equations 4–8 numerically, but the relationship between the DC bias voltage V_{dc} and the frequency shift Δf cannot be understood analytically.

Therefore, assuming that the vibration amplitude of the cantilever is very small compared to the length of the electrostatic force interaction region, we can obtain the analytical relationship between V_{dc} and the frequency shift Δf. The gradient of the electrostatic force is given by

$$\frac{dF_{ele}}{dz} = \frac{dF_{ele}(Q)}{dQ}\frac{dQ}{dV_s}\frac{dV_s}{dz}. \tag{50}$$

From Equations 24 and 33 and the relationship $C_g = \varepsilon_0/z$, dV_s/dz is given by

$$\frac{dV_s}{dz} = \frac{Q_s + Q_{it}}{\varepsilon_0} \tag{51}$$

and

$$\frac{dV_s}{dz} = \frac{Q_s}{\varepsilon_0} \tag{52}$$

for low- and high-frequency AC bias voltages, respectively. From Equations 22, 24, 31, and 33, the frequency shift of the electrostatic force is given by

$$\begin{aligned}\Delta f_L(0) &= -\frac{f_0}{2k}\frac{dF_{ele}(Q)}{dQ}\frac{dQ}{dV_s}\frac{dV_s}{dz} \\ &= -\frac{f_0}{2k}\frac{1}{\varepsilon_0^2}(C_D + C_{it})(Q_s + Q_{it})^2 \\ &= -\frac{f_0}{2k}\frac{C_g^2}{\varepsilon_0^2}(C_D + C_{it})(V_s - V_{dc})^2\end{aligned} \tag{53}$$

and

$$\begin{aligned}\Delta f_H(0) &= -\frac{f_0}{2k}\frac{dF_{ele}(Q)}{dQ}\frac{dQ}{dV_s}\frac{dV_s}{dz} = -\frac{f_0}{2k}\frac{1}{\varepsilon_0^2}C_D Q_s^2 \\ &= -\frac{f_0}{2k}\frac{C_g^2}{\varepsilon_0^2}C_D(V_s - V_{dc})^2\end{aligned} \tag{54}$$

for low- and high-frequency AC bias voltages, respectively. As shown in Equations 36–38, C_D in the charge depletion region is very different from C_D in the charge accumulation and charge inversion regions. Thus, these equations suggest that the Δf_L–V_{dc} curve for a low-frequency AC bias voltage is almost parabolic with respect to V_{dc} when $C_D < C_{it}$, while the Δf_H–V_{dc} curve for a high-frequency AC bias voltage is divided into three regions with respect to V_{dc}. These analytical equations do not necessarily quantitatively agree with the experimental results because they approximate small cantilever vibration amplitudes, but they can qualitatively explain the behavior of Δf–V_{dc} curves.

Experimental

Figure 4 shows the block diagram of AFM and high–low KPFS using AC bias voltages with high and low frequencies. The FM method was used to detect the tip–sample interaction force. The cantilever displacement signal measured using the displacement detection system was controlled by an automatic gain control (AGC) circuit to keep the cantilever vibration amplitude A constant, and the frequency shift Δf of the cantilever was measured using a phase-locked loop (PLL) circuit (SPECS GmbH: Nanonis OC4). AFM measurements were performed by controlling the tip–sample distance so that the frequency shift of the cantilever (Δf_{set}) was constant. In the low KPFS measurement using a low-frequency AC bias, the AC bias voltage $V_{ac}\cdot\cos 2\pi f_m t$ was generated by an oscillator. In contrast, in the high KPFS measurement using a high-frequency AC bias voltage, the signal $\cos 2\pi(2f_0)t$, which is a signal of twice the frequency synchronized with the cantilever vibration signal $\cos 2\pi f_0 t$, was generated by a PLL circuit with a narrow bandwidth and a doubler (amplitude modulator for second-harmonic generation) (Zurich Instruments: HF2LI-PLL and HF2LI-MOD). By mixing this signal and the signal from the oscillator $\cos 2\pi f_m t$ in a single-sideband (SSB) modulator (Zurich Instruments: HF2LI-MOD), the AC bias signal $V_{ac}\cdot\cos 2\pi(2f_0 + f_m)t$ was generated. The bias voltage, which is the sum of the DC bias voltage V_{dc} and the AC bias voltage ($V_{ac}\cdot\cos 2\pi f_m t$ or $V_{ac}\cdot\cos 2\pi(2f_0 + f_m)t$), was applied to the tip, and the ground was connected to the sample. The modulation component of the frequency shift of the cantilever $\Delta f(f_m)$ was detected using a lock-in amplifier (Zurich Instruments: HF2LI). Bias spectral data were obtained by measuring $\Delta f(f_m)$ and Δf as a function of the DC bias voltage V_{dc} while keeping the distance between the tip and the sample constant. These experiments were performed in a vacuum environment using a JEOL scanning probe microscope (JEOL: JSPM-4210).

A silicon substrate patterned with n- and p-type impurities was used as a semiconductor sample [22,27,28]. Figure 5 shows the dopant pattern of the silicon substrate used in the measurements and the impurity concentrations. As shown in Figure 5,

Figure 4: Block diagram of AFM and high–low KPFS. In low KPFS, a signal V_{ac}·cos $2\pi f_m t$ is generated by the oscillator. In high KPFS, a signal cos $2\pi(2f_0)t$ of twice the resonance frequency synchronized with the cantilever oscillation is generated by the PLL and the doubler, and a signal V_{ac}·cos $2\pi(2f_0 + f_m)t$ is generated by mixing the signal cos $2\pi(2f_0)t$ and the signal cos $2\pi f_m t$ in the SSB modulator. The figure was adapted from [20] (© 2020 Y. Sugawara et al., published by IOP Publishing Ltd., distributed under the terms of the Creative Commons Attribution 4.0 International License, https://creativecommons.org/licenses/by/4.0)

the silicon substrate has three types of impurity regions: an n-type region, a p-type region, and an n^+-type region. The impurity concentrations of the n, p, and n^+ regions are 1×10^{15} cm^{-3}, 2×10^{16} cm^{-3}, and 5×10^{19} cm^{-3}, respectively.

Figure 5: Schematic of the silicon substrate with three types of impurity pattern, that is, n-, p-, and, n^+-type regions, used for the measurement.

As a force sensor, a PtIr-coated conductive cantilever (NanoWorld: NCHPt) was used. The resonance frequency f_0, force constant k, and Q of the PtIr-coated cantilever were 292.68 kHz, 42 N/m, and 8406, respectively.

The cantilever oscillation amplitude for the high–low KPFS measurement was set to A = 10 nm throughout the experiment. The AC bias voltage was V_{ac} = 0.5 V, and the modulation frequencies of the AC bias voltage in high KPFS and low KPFS were $2f_0 + f_m$ = 542.3 kHz and f_m = 100 Hz, respectively.

Results and Discussion

First, we performed AFM/KPFM measurements on the pn-patterned Si surface to identify the dopant regions on the semiconductor surface. Figure 6a and Figure 6b show the topographic and CPD images of the pn-patterned Si substrate, respectively. The CPD image in Figure 6b was obtained by KPFM using an AC bias voltage with a low modulation frequency of f_m = 100 Hz. Figure 6c and Figure 6d show the line profiles corresponding to the white lines in Figure 6a and Figure 6b, respectively. From the topographic image and the line profile, there are rodlike protrusions on the surface with a width of approximately 1 µm and a height of approximately 60 nm. Compared with the data of the pn-patterned Si substrate in Figure 5, these rodlike protrusions correspond to p-type or n-type regions, and the low areas between the rodlike protrusions correspond to n^+-type regions. From the CPD image and the line profile, there is a difference of approximately 30–40 mV between the CPD values of the two rodlike protrusions; the region with the highest CPD value is the p-type region, the region with a CPD value 30–40 mV below the highest value is the n-type region, and the region with the lowest CPD value is the n^+-type region. From these CPD values, the n^+-, n-, and p-type regions can be assigned as shown in Figure 6d [22,27,28].

Next, we performed high–low KPFS experiments at the center point in the n-type region shown in Figure 6a. Figure 7a shows

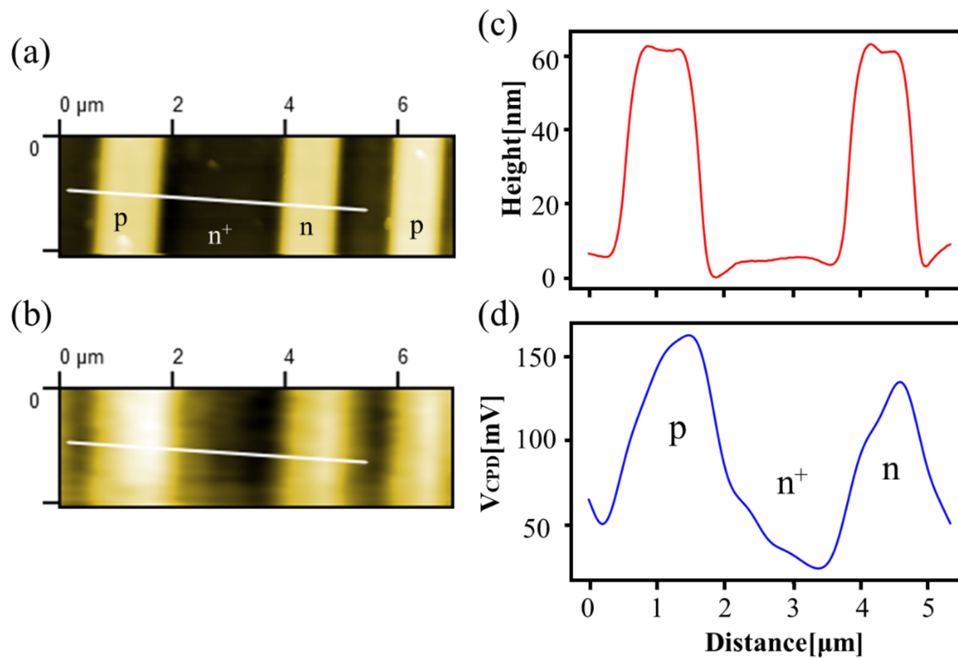

Figure 6: (a) Surface topography and (b) CPD image of the pn-patterned Si surface. The CPD image was obtained by KPFM using an AC bias voltage with a low modulation frequency of f_m = 100 Hz. The scan size was 7 µm × 2.1 µm. (c) Line profile corresponding to the white line in panel (a); (d) line profile corresponding to the white line in panel (b).

the dependence of the modulation component of the frequency shift $\Delta f(f_m)$ on the DC bias voltage V_{dc} in high–low KPFS ($\Delta f(f_m)$–V_{dc} curves). Since the coefficients in Equations 43 and 44 for high KPFS are 1/2 compared with those in Equation 30 for low KPFS, the modulation component of the frequency shift $\Delta f(f_m)$ in high KPFS is doubled. The tip–sample distance was fixed at Δf_{set} = −300 Hz ($z_{to} \approx$ 15 nm) as the frequency shift set point when the DC bias voltage V_{dc} = 3 V and the AC bias voltage with amplitude V_{ac} = 0.5 V were applied. In low KPFS, the $\Delta f(f_m)$–V_{dc} curve shows an almost linear behavior with respect to V_{dc} from −3.5 V to +3.5 V. In contrast, in high KPFS, the $\Delta f(f_m)$–V_{dc} curve does not show a linear behavior with respect to V_{dc} and is roughly divided into three regions: (i) −3.5 V to −0.5 V, (ii) −0.5 V to +0.5 V, and (iii) +0.5 V to +3.5 V. The slope of the curve is larger in regions (i) and (iii) and smaller in region (ii). These experimental results on the $\Delta f(f_m)$–V_{dc} curves in Figure 7a agree well with the theoretical expectation that the $\Delta f_L(f_m)$–V_{dc} curve for low-frequency AC bias voltages is nearly linear with respect to V_{dc} with slope $C_D + C_{it}$ and that the $\Delta f_H(f_m)$–V_{dc} curve for high-frequency AC bias voltages is divided into three regions with respect to V_{dc} with slopes of C_D in the charge depletion region and of C_g in the charge accumulation and charge inversion regions. A similar result that the $\Delta f(f_m)$–V_{dc} curve is divided into three regions has already been observed in organic semiconductor samples by Schumacher and co-workers [29].

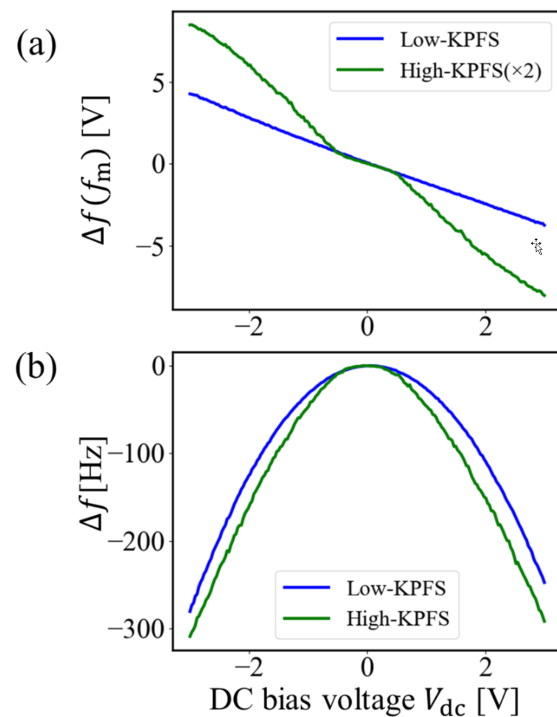

Figure 7: (a) $\Delta f(f_m)$–V_{dc} curves and (b) Δf–V_{dc} curves obtained on the n-type Si surface. The tip–sample distance was set with Δf_{set} = −300 Hz ($z_{to} \approx$ 15 nm) when V_{dc} = 3 V and V_{ac} = 0.5 V were applied between the tip and the sample.

The DC bias voltages that reduced $\Delta f(f_m)$ to zero are slightly different depending on the frequency of the AC bias voltage: $V_{s(LF)} \approx 47.5$ mV and $V_{s(HF)} \approx 12.0$ mV for low- and high-frequency AC bias voltages, respectively. The difference between $V_{s(LF)}$ and $V_{s(HF)}$ is $\Delta V_s = -35.5$ mV, which indicates that the interface band is bent downward in the n-type region, suggesting the presence of donor-like interface states [22].

Figure 7b shows the dependence of the frequency shift Δf on DC bias voltage V_{dc} in high–low KPFS (Δf–V_{dc} curves) simultaneously measured with Figure 7a. The Δf–V_{dc} curve is almost parabolic for the low-frequency AC bias voltage. In contrast, the Δf–V_{dc} curve for the high-frequency AC bias voltage is highly distorted from parabolic, especially in the V_{dc} range of −3.5 V to −0.5 V (the charge accumulation region) and +0.5 V to +3.5 V (the charge inversion region). These experimental results on the Δf–V_{dc} curves in Figure 7b also agree well with the theoretical expectation that the Δf–V_{dc} curve is almost parabolic for low-frequency AC bias voltages, while it is divided into three regions with respect to V_{dc} for high-frequency AC bias voltages.

This is the first observation of the phenomenon in which the $\Delta f(f_m)$–V_{dc} and Δf–V_{dc} curves are highly dependent on the frequency of the applied AC bias voltage. These results experimentally show that carrier transport between the bulk and interface states of a semiconductor sample is strongly affected by the frequency of the AC bias voltage and that there is indeed a difference between the low-frequency tip–sample capacitance (C_{LF}) and the high-frequency tip–sample capacitance (C_{HF}).

Next, we performed high–low KPFS measurements at the same measurement points as in Figure 7, varying the tip–sample distance. Figure 8a and Figure 8b show the measured $\Delta f(f_m)$–V_{dc} curves when the tip–sample distance was fixed with $\Delta f_{set} = -200$ Hz ($z_{to} \approx 23$ nm) and $\Delta f_{set} = -100$ Hz ($z_{to} \approx 40$ nm), respectively, as the frequency shift set point. The DC bias voltage $V_{dc} = 3$ V and the AC bias voltage $V_{ac} = 0.5$ V were the same as those used in the case of Figure 7. The modulation component of the frequency shift $\Delta f(f_m)$ in high KPFS was doubled. Similarly, Figure 8c and Figure 8d show the Δf–V_{dc} curves at $\Delta f_{set} = -200$ Hz ($z_{to} \approx 23$ nm) and $\Delta f_{set} = -100$ Hz ($z_{to} \approx 40$ nm) simultaneously measured with Figure 8a and Figure 8b, respectively.

The $\Delta f(f_m)$–V_{dc} curves in low KPFS show an almost linear behavior at both tip–sample distances. In contrast, the $\Delta f(f_m)$–V_{dc} curves in high KPFS do not show a linear behavior and are roughly divided into three regions. The $\Delta f(f_m)$–V_{dc} curves in high KPFS show that the DC bias voltage region (ii) corresponding to the charge depletion region becomes wider from −1.5 V to +1.5 V (Figure 8a) and from −3.3 V to +3.3 V (Figure 8b) as the tip–sample distance increases. The wider voltage region (ii) is due to the smaller ratio of the DC bias

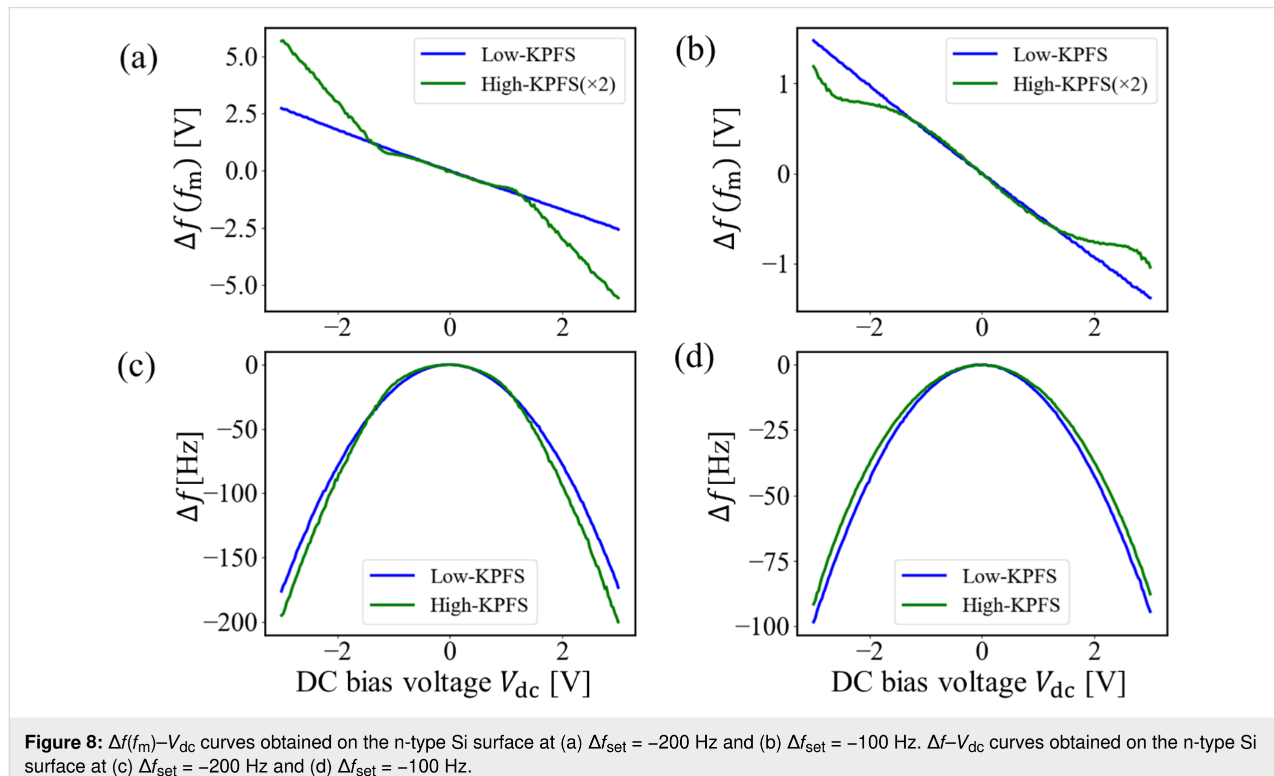

Figure 8: $\Delta f(f_m)$–V_{dc} curves obtained on the n-type Si surface at (a) $\Delta f_{set} = -200$ Hz and (b) $\Delta f_{set} = -100$ Hz. Δf–V_{dc} curves obtained on the n-type Si surface at (c) $\Delta f_{set} = -200$ Hz and (d) $\Delta f_{set} = -100$ Hz.

voltage divided inside the semiconductor. Furthermore, as the tip–sample distance increases, the Δf–V_{dc} curves become nearly parabolic not only for low-frequency AC bias voltages but also for high-frequency AC bias voltages. The reason why the Δf–V_{dc} curve for high-frequency AC bias voltages becomes almost parabolic as the tip–sample distance increases is because the range of the DC bias voltage corresponding to the charge depletion region is extended.

We also performed high–low KPFS measurements at the center point in the p-type region in Figure 6a. Figure 9a and Figure 9b show the measured $\Delta f(f_m)$–V_{dc} curves and Δf–V_{dc} curves, respectively. The tip–sample distance was fixed with Δf_{set} = −200 Hz (z_{to} ≈ 23 nm) as the frequency shift set point when the DC bias voltage V_{dc} = 3 V and the AC bias voltage with amplitude V_{ac} = 0.5 V were applied. In Figure 9a, the $\Delta f(f_m)$–V_{dc} curve in low KPFS shows an almost linear behavior from −3.5 V to +3.5 V, while the $\Delta f(f_m)$–V_{dc} curve in high KPFS is roughly divided into three regions: (i) −3.5 V to −1.5 V, (ii) −1.5 V to +1.5 V, and (iii) +1.5 V to +3.5 V. The slope of the curve is larger in regions (i) and (iii) and smaller in region (ii). The DC bias voltages that reduced $\Delta f(f_m)$ to zero were estimated to be $V_{s(LF)}$ ≈ 169.4 mV and $V_{s(HF)}$ ≈ 143.3 mV for low- and high-frequency AC bias voltages, respectively. The difference between $V_{s(LF)}$ and $V_{s(HF)}$ is ΔV_s = −25.1 mV. This indicates that the interface band is bent downward in the p-type region, consistent with the previous high–low KPFM results [22].

Furthermore, in Figure 9b, the Δf–V_{dc} curve is almost parabolic for the low-frequency AC bias voltage, whereas it is highly distorted from parabolic for the high-frequency AC bias voltage. Thus, the $\Delta f(f_m)$–V_{dc} and Δf–V_{dc} curves measured in the p-type region are highly dependent on the frequency of the applied AC bias voltage, which is in good agreement with those measured in the n-type region as well as the theoretical prediction.

The dependence of the $\Delta f(f_m)$–V_{dc} and Δf–V_{dc} curves on the frequency of the AC bias voltage is due to the dependence on the contribution of the capacitance C_{it} caused by the interface states to the electrostatic force. In other words, when a low-frequency AC bias is used, the capacitance inside the semiconductor is given by the sum of the depletion layer capacitance C_D and the capacitance C_{it} due to the interface states according to Equation 30. In contrast, when a high-frequency AC bias is used, the depletion layer capacitance C_D or the gap capacitance C_g has a significant effect on the electrostatic force because the capacitance C_{it} due to the interface states makes no contribution to the electrostatic force according to Equations 43 and 44.

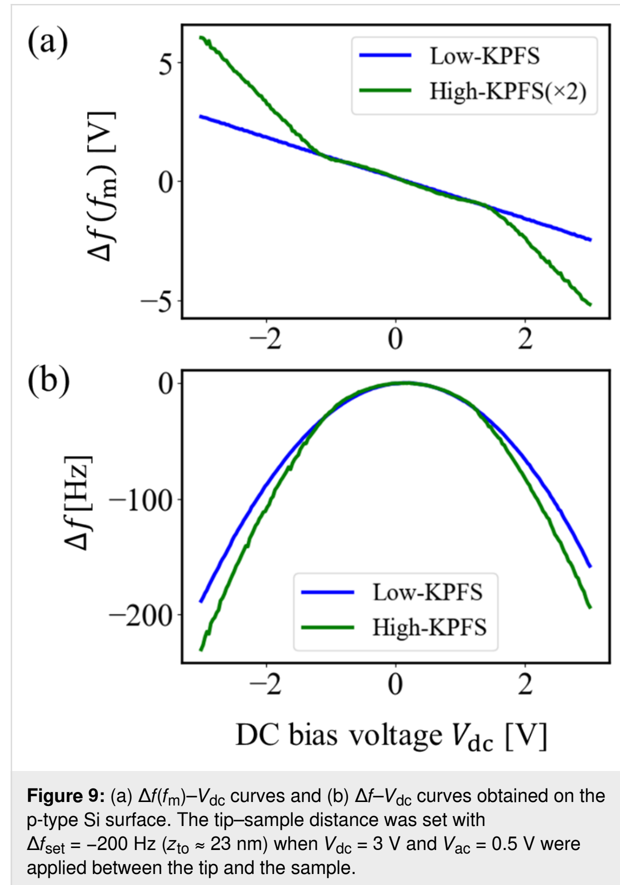

Figure 9: (a) $\Delta f(f_m)$–V_{dc} curves and (b) Δf–V_{dc} curves obtained on the p-type Si surface. The tip–sample distance was set with Δf_{set} = −200 Hz (z_{to} ≈ 23 nm) when V_{dc} = 3 V and V_{ac} = 0.5 V were applied between the tip and the sample.

Finally, we estimated the interface state density D_{it} in the n-type region on the pn-patterned Si surface using the measured $\Delta f(f_m)$–V_{dc} curve in Figure 7a for the closest distance between the tip and the surface. In depletion region (ii), the slope of the $\Delta f(f_m)$–V_{dc} curve in low KPFS is slightly larger than that in high KPFS. From Equations 30 and 43, at V_{dc} = −0.3 V, the capacitances per unit area inside the semiconductor were estimated to be $C_D + C_{it} \simeq 3.41 \times 10^{-23}$ F/cm^2 in low KPFS and $C_D \simeq 2.94 \times 10^{-23}$ F/cm^2 in high KPFS. The parameters used in the estimations of the interface state density were the same as those used in the experiments (f_0 = 292.68 kHz, k = 42 N/m, and V_{ac} = 0.5 V). The average distance between the tip and the surface was assumed to be $z_{t0} \simeq 15$ nm. Hence, the capacitance per unit area due to the surface states was estimated to be $C_{it} \simeq 4.67 \times 10^{-24}$ F/cm^2. From Equation 48, the interface state density was calculated to be $D_{it} \simeq 1.82 \times 10^{14}$ cm^{-2} eV at V_{dc} = −0.3 V. This value is reasonable for the interface state density on the pn-patterned Si surface. This is the first estimate of the interface state density using the high–low KPFS method and demonstrates the usefulness of high–low KPFS.

Conclusion

In this study, we proposed high-low KPFS using high-frequency and low-frequency AC bias voltages to measure the inter-

face state density in semiconductors. We derived an analytical expression for the electrostatic force between the tip and the sample that takes into account the charge transfer between the bulk and interface states in the semiconductor. From the analytical equation, we found that the slopes of the $\Delta f(f_m)$–V_{dc} curves for low- and high-frequency AC bias voltages depend on the capacitances $C_D + C_{it}$ and C_D between the tip and the sample, respectively. We also showed that the analysis of the difference between $C_D + C_{it}$ and C_D for low- and high-frequency AC bias voltages provides information on the interface state density D_{it} in the semiconductor bandgap.

Experimentally, $\Delta f(f_m)$–V_{dc} and Δf–V_{dc} curves were measured for impurity-doped Si samples (n- and p-types). When a low-frequency AC bias voltage was used, the $\Delta f(f_m)$–V_{dc} curves were almost linear, and the Δf–V_{dc} curves were almost parabolic. In contrast, when a high-frequency AC bias voltage was used, the $\Delta f(f_m)$–V_{dc} curves were not linear but roughly divided into three regions, and the Δf–V_{dc} curves were distorted from a parabolic shape. These differences were due to the dependence on the contribution of the capacitance C_{it} caused by the interface states to the electrostatic force. That is, when a low-frequency AC bias voltage is used, the capacitance inside the semiconductor is given by the sum of the capacitance C_{it} caused by the interface states and the depletion layer capacitance C_D. In contrast, when a high-frequency AC bias is used, the contribution of the capacitance C_{it} due to the interface states is almost negligible, and the depletion layer capacitance C_D has a large influence on the electrostatic force. In the depletion region, the slope of the $\Delta f(f_m)$–V_{dc} curve for a low-frequency AC bias was found to be slightly larger than that for a high-frequency AC bias. We demonstrated for the first time that the interface state density D_{it} could be estimated from the difference in these slopes.

The experimental result that the Δf–V_{dc} curves highly depend on the frequency of the applied AC bias voltage strongly suggests the feasibility of a new spectroscopy method to measure the frequency dependence of carrier transfer in a sample. That is, in this high-low KPFS, only f_m or $2f_0 + f_m$ was used as the frequency of the AC bias voltage, but AC bias voltages with frequencies other than these can be applied to measure Δf–V_{dc} curves. Therefore, note that the measurement of the Δf–V_{dc} curve can be applied for AC bias voltages with very high frequencies, such as in the microwave region, which are not applicable in the conventional KPFM and KPFS.

In the future, high–low KPFS measurements with 2D scanning of the tip on the sample surface are expected to enable measurement of the local interface state density of the sample surface on the nanoscale. Therefore, the high–low KPFS method proposed in this study is expected to be widely used for sensitive and high-resolution nanoscale measurements of impurity concentration and defect level distributions at the surfaces and interfaces of various semiconductor materials and devices.

Funding

This work was supported by JSPS KAKENHI Grant Numbers JP21H04662, JP22H00282, JP22K18946, and JP22K18970.

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References

1. Reed, M. L.; Plummer, J. D. *J. Appl. Phys.* **1988,** *63,* 5776–5793. doi:10.1063/1.340317
2. Engel-Herbert, R.; Hwang, Y.; Stemmer, S. *J. Appl. Phys.* **2010,** *108,* 124101. doi:10.1063/1.3520431
3. Guo, Y.; Wei, X.; Shu, J.; Liu, B.; Yin, J.; Guan, C.; Han, Y.; Gao, S.; Chen, Q. *Appl. Phys. Lett.* **2015,** *106,* 103109. doi:10.1063/1.4914968
4. Sadewasser, S.; Glatzel, T., Eds. *Kelvin Probe Force Microscopy: From Single Charge Detection to Device Characterization;* Springer Series in Surface Sciences, Vol. 65; Springer, 2018. doi:10.1007/978-3-319-75687-5
5. Melitz, W.; Shen, J.; Kummel, A. C.; Lee, S. *Surf. Sci. Rep.* **2011,** *66,* 1–27. doi:10.1016/j.surfrep.2010.10.001
6. Binnig, G.; Quate, C. F.; Gerber, C. *Phys. Rev. Lett.* **1986,** *56,* 930–933. doi:10.1103/physrevlett.56.930
7. Giessibl, F. J. *Rev. Mod. Phys.* **2003,** *75,* 949–983. doi:10.1103/revmodphys.75.949
8. Albrecht, T. R.; Grütter, P.; Horne, D.; Rugar, D. *J. Appl. Phys.* **1991,** *69,* 668–673. doi:10.1063/1.347347
9. Fernández Garrillo, P. A.; Grévin, B.; Chevalier, N.; Borowik, Ł. *Rev. Sci. Instrum.* **2018,** *89,* 043702. doi:10.1063/1.5007619
10. Khoussa, H.; Baris, B.; Alchaar, M.; Chaumeton, F.; Ghamnia, M.; Gauthier, S.; Martrou, D. *Phys. Status Solidi B* **2018,** *255,* 1700482. doi:10.1002/pssb.201700482
11. Ma, Z. M.; Kou, L.; Naitoh, Y.; Li, Y. J.; Sugawara, Y. *Nanotechnology* **2013,** *24,* 225701. doi:10.1088/0957-4484/24/22/225701
12. Glatzel, T.; Sadewasser, S.; Shikler, R.; Rosenwaks, Y.; Lux-Steiner, M. C. *Mater. Sci. Eng., B* **2003,** *102,* 138–142. doi:10.1016/s0921-5107(03)00020-5
13. Rosenwaks, Y.; Shikler, R.; Glatzel, T.; Sadewasser, S. *Phys. Rev. B* **2004,** *70,* 085320. doi:10.1103/physrevb.70.085320
14. Wen, H. F.; Li, Y. J.; Arima, E.; Naitoh, Y.; Sugawara, Y.; Xu, R.; Cheng, Z. H. *Nanotechnology* **2017,** *28,* 105704. doi:10.1088/1361-6528/aa5aef
15. Zou, S.; Yokoyama, H.; Sugawara, Y.; Li, Y. J. *J. Phys. Chem. C* **2020,** *124,* 21641–21645. doi:10.1021/acs.jpcc.0c07488
16. Barth, C.; Henry, C. R. *Nanotechnology* **2006,** *17,* S155–S161. doi:10.1088/0957-4484/17/7/s09
17. Barth, C.; Henry, C. R. *J. Phys. Chem. C* **2009,** *113,* 247–253. doi:10.1021/jp807340k
18. Polak, L.; Wijngaarden, R. J. *Phys. Rev. B* **2016,** *93,* 195320. doi:10.1103/physrevb.93.195320

19. Arita, M.; Torigoe, K.; Yamauchi, T.; Nagaoka, T.; Aiso, T.; Yamashita, Y.; Motooka, T. *Appl. Phys. Lett.* **2014,** *104,* 132103. doi:10.1063/1.4870419
20. Sugawara, Y.; Miyazaki, M.; Li, Y. J. *J. Phys. Commun.* **2020,** *4,* 075015. doi:10.1088/2399-6528/aba477
21. Izumi, R.; Li, Y. J.; Naitoh, Y.; Sugawara, Y. *Microscopy (Oxford, U. K.)* **2022,** *71,* 98–103. doi:10.1093/jmicro/dfab055
22. Dâna, A.; Yamamoto, Y. *Nanotechnology* **2005,** *16,* S125–S133. doi:10.1088/0957-4484/16/3/023
23. Hudlet, S.; Saint Jean, M.; Roulet, B.; Berger, J.; Guthmann, C. *J. Appl. Phys.* **1995,** *77,* 3308–3314. doi:10.1063/1.358616
24. Sze, S. M.; Ng, K. K. Metal-Insulator-Semiconductor Capacitors. In *Physics of semiconductor devices,* 3rd ed.; Sze, S. M.; Ng, K. K., Eds.; John Wiley & Sons, 2006; pp 197–240. doi:10.1002/9780470068328.ch4
25. Selberherr, S. *The Physical Parameters;* Analysis and Simulation of Semiconductor Devices; Springer Vienna: Vienna, Austria, 1984; pp 80–126. doi:10.1007/978-3-7091-8752-4_4
26. Schroder, D. K. Carrier Lifetimes. In *Semiconductor material and device characterization;* Schroder, D. K., Ed.; John Wiley & Sons, 2005; pp 389–464. doi:10.1002/0471749095.ch7
27. Sugimura, H.; Ishida, Y.; Hayashi, K.; Takai, O.; Nakagiri, N. *Appl. Phys. Lett.* **2002,** *80,* 1459–1461. doi:10.1063/1.1455145
28. Nakagiri, N.; Sugimura, H.; Ishida, Y.; Hayashi, K.; Takai, O. *Surf. Sci.* **2003,** *532-535,* 999–1003. doi:10.1016/s0039-6028(03)00456-4
29. Schumacher, Z.; Rejali, R.; Cowie, M.; Spielhofer, A.; Miyahara, Y.; Grutter, P. *ACS Nano* **2021,** *15,* 10377–10383. doi:10.1021/acsnano.1c02600

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